VA600-RTM
User Manual

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1 Introduction

The VA600-RTM is a 6U VPX RTM for the ADK-VA600 6U Space VPX reference platform. It has high-speed and low-speed IO breakout for the Versal board, as well as it's own Zynq MPSoC FPGA connected to the Versal SMAP interface

1.1 Key Features

Key Features

- 6U VPX RTM with Zynq MPSoC for Versal SMAP control.
- **Versal Debug Interfaces**:
  - USB to UART converter
  - USB to JTAG converter
  - ADM SmartLynq+ compatible High-Speed Debug Port (HSDP).
  - RS-232 DB-9 serial output
- **Versal IO Interfaces**:
  - 8 8Gbps MGT lanes to two SF-8644 connectors
  - 3 10Gbps MGT lanes to three SFP+ connectors
  - 8 10Gbps MGT lanes to two Samtec FireFly connectors
  - Two SpaceWire interfaces
  - Gigabit Ethernet Port
  - External reference clock input
  - 40 Singled Ended GPIO
  - CAN Bus interface to GPIO connector
- **On-Board Zynq MPSoC**:
  - 4GB PS DDR4
  - 37 GPIOs to the FPGA fabric, enough to allow SMAP Passthrough
  - USB to UART converter
  - SD Card boot device
  - Gigabit Ethernet interface to PS
  - USB interface to PS
  - I2C/sideband signal connections to on-board transceivers
  - I2C interface to VPX backplane
  - 4 User controllable LEDs
  - 4 User controllable switches
  - On-Board voltage monitoring
  - Weight: 224g

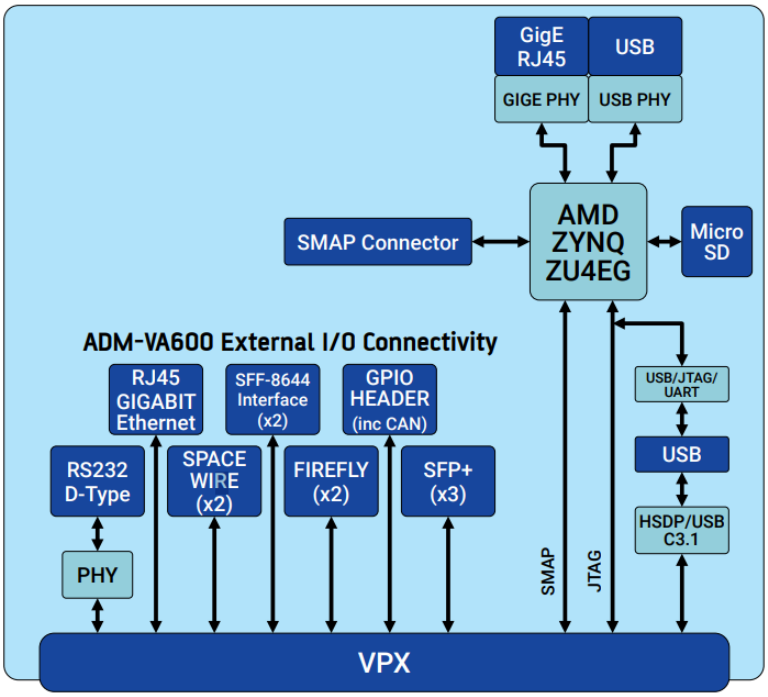


Figure 1 : VA600-RTM Block Diagram

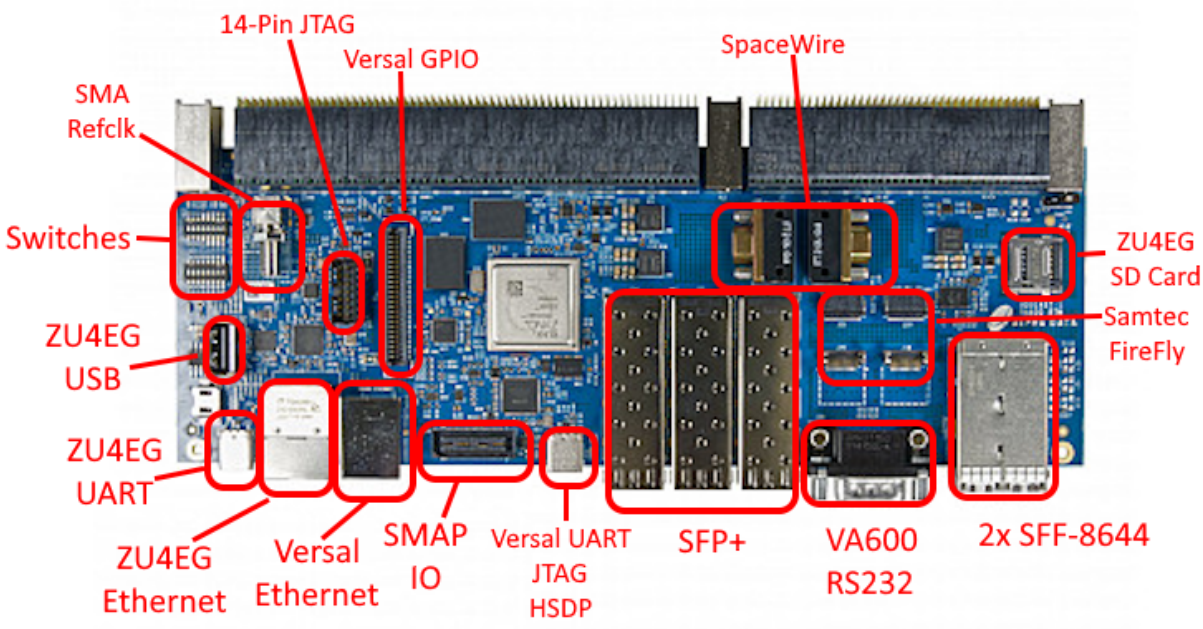


Figure 2 : VA600-RTM Board Diagram

2 Installation

2.1 Hardware Installation

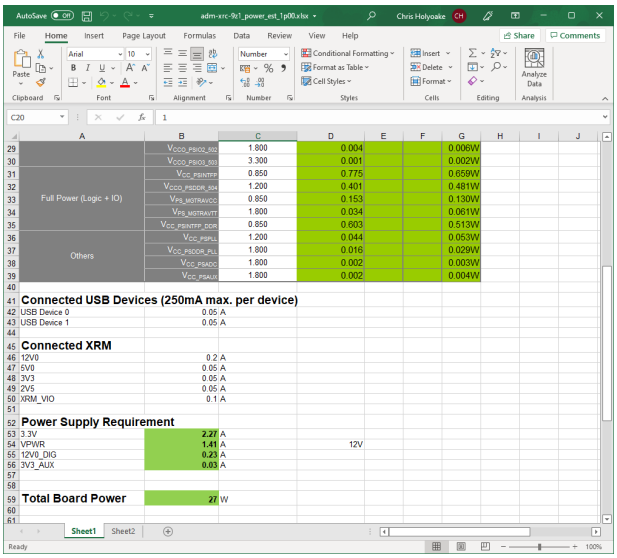
2.1.1 Handling Instructions

The components on this board can be damaged by electrostatic discharge (ESD). To prevent damage, observe ESD precautions:

- Always wear a wrist-strap when handling the card
- Hold the board by the edges
- Avoid touching any components
- Store in ESD safe bag.

2.1.2 Cooling Requirements

The power dissipation of the board is highly dependent on the FPGA application. A power estimator spreadsheet is available on request from Alpha Data. This should be used in conjunction with Xilinx power estimation tools to determine the exact current requirements for each power rail.



	A	B	C	D	E	F	G	H	I	J
29		$V_{CCO\_PSIO2\_502}$	1.800	0.004			0.006W			
30		$V_{CCO\_PSIO1\_501}$	3.300	0.001			0.002W			
31		$V_{CC\_PSINTFP}$	0.850	0.775			0.659W			
32		$V_{CCO\_PSDDR\_504}$	1.200	0.401			0.481W			
33	Full Power (Logic + IO)	$V_{PS\_MGTRAVCC}$	0.850	0.153			0.130W			
34		$V_{PS\_MGTRAVTT}$	1.800	0.034			0.061W			
35		$V_{CC\_PSINTFP\_DDR}$	0.850	0.603			0.513W			
36		V_{CC_PSPLL}	1.200	0.044			0.053W			
37	Others	$V_{CC\_PSDDR\_PLL}$	1.800	0.016			0.029W			
38		V_{CC_PSADC}	1.800	0.002			0.003W			
39		V_{CC_PSAUX}	1.800	0.002			0.004W			
40										
41	**Connected USB Devices (250mA max. per device)**									
42	USB Device 0	0.05 A								
43	USB Device 1	0.05 A								
44										
45	**Connected XRM**									
46	12V0	0.2 A								
47	5V0	0.05 A								
48	3V3	0.05 A								
49	2V5	0.05 A								
50	XRM_VIO	0.1 A								
51										
52	**Power Supply Requirement**									
53	3.3V	2.27 A								
54	VPWR	1.41 A		12V						
55	12V0_DIG	0.23 A								
56	3V3_AUX	0.03 A								
57										
58										
59	**Total Board Power**	27 W								
60										
61										

Figure 3 : Alpha Data Power Estimator Spreadsheet

3 Functional Description

3.1 Overview

3.1.1 Switch Definitions

There are two sets of eight DIP switches (16 switches in total) placed on the top of the board. Some switch states can be controlled using the FPGA IO. These signals are shown in the corresponding table.

The default switch states for SD card boot mode are SW2[8:1]:00000000 and SW1[8:1]:00001100.

Switch Ref.	Function	FPGA Pin	ON State	Off State
SW2-1	VA600 UART RS485 TE	K17	VA600 UART RS485 Termination Enabled	VA600 RS485 Termination Disabled
SW2-2	VA600 UART RS485 EN	J17	VA600 UART RS485 Mode	VA600 UART RS232 Mode
SW2-3	Bypass ZU4EG JTAG	-	ZU4EG removed from JTAG chain	ZU4EG included in JTAG chain
SW2-4	Bypass VPX JTAG	-	VPX Backplane removed from JTAG chain	VPX Backplane included in JTAG chain
SW2-5	VA600 USB-to-UART EN	-	VA600 USB-to-UART enabled (RS232/485 disabled)	VA600 USB-to-UART disabled (RS232/485 enabled)
SW2-6	ZU4EG Reset	-	ZU4EG held reset active	ZU4EG held reset cleared
SW2-7	VPX SYSRESET	-	VPX SYSRESET active	VPX SYSRESET cleared
SW2-8	VPX POR EN	-	RTM drives power on reset to VPX_SYSRESET	Leaves VPX_SYSRESET floating

Table 1 : SW2 Switch Definitions

Switch Ref.	Function	FPGA Pin	ON State	Off State
SW1-1	BootMode 0	-	See Table 11	
SW1-2	BootMode 1	-	See Table 11	
SW1-3	BootMode 2	-	See Table 11	
SW1-4	BootMode 3	-	See Table 11	
SW1-5	User switch 1	B11	FPGA Pin High	FPGA Pin Low
SW1-6	User switch 2	A10	FPGA Pin High	FPGA Pin Low
SW1-7	User switch 3	A12	FPGA Pin High	FPGA Pin Low
SW1-8	User switch 4	A11	FPGA Pin High	FPGA Pin Low

Table 2 : SW1 Switch Definitions

3.1.2 LED Definitions

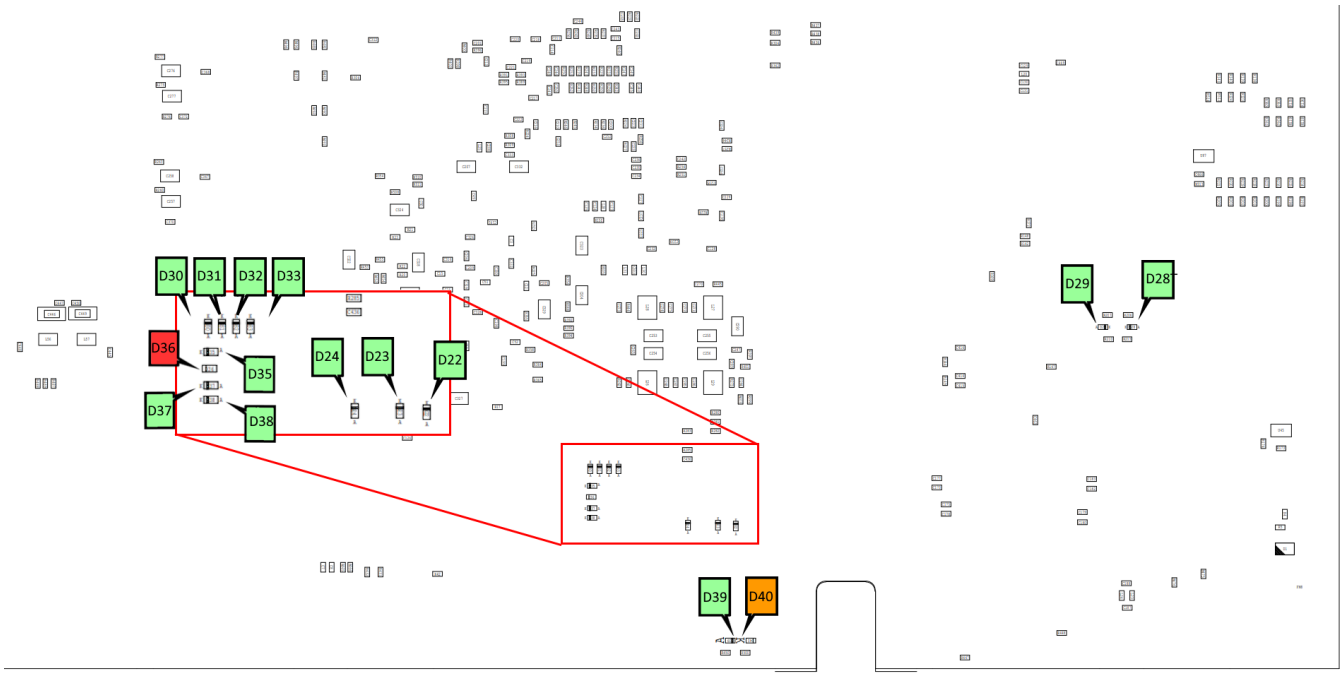


Figure 4 : LED Locations on Bottom of Board

Comp. Ref.	Function	ON State	Off State
D38(Green)	Power OK	Power supplies in range	Power supplies not in range
D37(Green)	ZU4 PS Done	ZU4 FPGA configured	ZU4 FPGA not configured
D35(Green)	ZU4 PS Error Status Pin	PS Error Status Asserted	PS Error Status Deasserted
D36(Red)	ZU4 PS Error Pin	PS Error Asserted	PS Error Deasserted
D39(Green)	VA600 Ethernet LED0	See VA600 User Guide	
D40(Amber)	VA600 Ethernet LED1	See VA600 User Guide	
D28(Green)	ZU4 UART RX Activity	Activity	No Activity
D29(Green)	ZU4 UART TX Activity	Activity	No Activity
D33(Green)	ZU4 Controlled LED 1	ZU4 Pin G1 High	ZU4 Pin G1 Low
D32(Green)	ZU4 Controlled LED 2	ZU4 Pin F1 High	ZU4 Pin F1 Low
D31(Green)	ZU4 Controlled LED 3	ZU4 Pin E1 High	ZU4 Pin E1 Low
D30(Green)	ZU4 Controlled LED 4	ZU4 Pin D1 High	ZU4 Pin D1 Low
D22(Green)	Versal Controlled LED 1	Versal Pin AR9 high	Versal Pin AR9 low
D23(Green)	Versal Controlled LED 2	Versal Pin AN8 high	Versal Pin AN8 low
D24(Green)	Versal Controlled LED 3	Versal Pin AP7 high	Versal Pin AP7 low

Table 3 : LED Definitions

3.2 Versal I/O

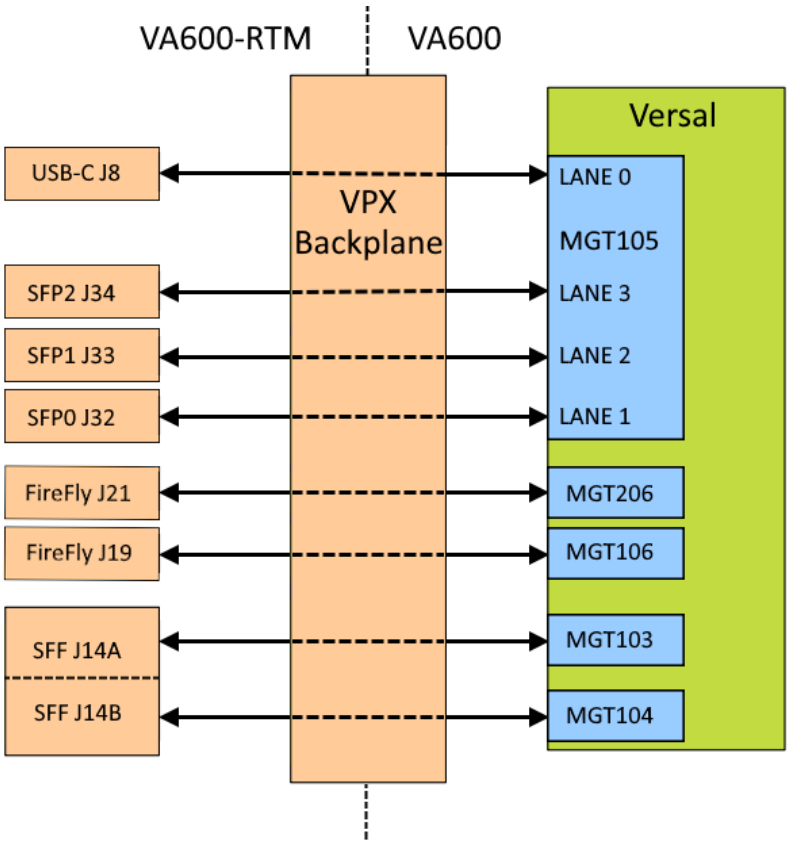


Figure 5 : Versal Transceivers

3.2.1 SFF-8644

A dual SFF-8644 connector is provided to break out VA600 MGT interfaces on banks 103 and 104. SFF J14A connects to bank 103 and J14B connects to bank 104. This can be used to bring out the VA600 PCIe over a cable.

The SFF-8644 interfaces connect to the ZU4EG PS I2C0 interface. Each SFF I2C interface has a bidirectional buffer with an enable control pin, controlled through PS MIO GPIO and PL GPIO. The pin should be driven high to enable the interface. The enables have a pull-down resistor so they can be undriven if unused. The pins to enable the SFF I2C interfaces are:

SFF Interface	PS Pin Name	PS Pin Number	PL Pin Number
SFF J14A	MIO12	AC17	J12
SFF J14B	MIO19	AE19	F10

Table 4 : SFF I2C Enables

To control the transceiver's I2C interface, see section: I2C Interface

3.2.2 SFP+

Three SFP+ cages are connected to VA600 MGT bank 105. SFP J32 connects to lane 1, SFP J33 connects to lane 2 and SFP J34 connects to lane 3. Lane 0 is used for the High-Speed Debug Port (HSDP).

The SFP I2C interfaces connect to the ZU4EG PS I2C0 interface. Each SFP I2C interface has a bidirectional buffer with an enable control pin, controlled through PS MIO GPIO. The pin should be driven high to enable the interface. The enables have a pull-down resistor so they can be undriven if unused. The pins to enable the SFP

I2C interfaces are:

Signal	PS Pin Name	PS Pin Number
SFP0 J32 I2C EN	MIO30	F16
SFP1 J33 I2C EN	MIO31	H16
SFP2 J34 I2C EN	MIO32	J16

Table 5 : SFP I2C Enables

To control the transceiver's I2C interface, see section: I2C Interface

3.2.3 FireFly

Two FireFly connectors are connected to VA600 MGT banks 106 and 206. FireFly 1 J19 connects to bank 106 and FireFly 2 J21 connects to bank 206. Each FireFly connector has the sideband signals: I2C_SDA, I2C_SCL, MODPRES_L, MODSEL_L, INT_L, RESET_L.

RESET_L and INT_L are common to both FireFly transceivers

Signal	PS Pin Name	PS Pin Number
I2C_SCL	MIO2	AF15
I2C_SDA	MIO3	AH15
INT_L	MIO11	AE17
RESET_L	MIO10	AD17
FireFly 1 J19 MODSEL_L	MIO34	L17
FireFly 1 J19 MODPRES_L	MIO35	H17
FireFly 2 J21 MODSEL_L	MIO24	AB19
FireFly 2 J21 MODPRES_L	MIO25	AB21

Table 6 : FireFly Sideband Signals

To control the transceiver's I2C interface, see section: I2C Interface

3.2.4 UART/RS232/RS485

The RS232/485 interface connects to the Versal pins LPD MIO17 (TX) and LDP MIO16 (RX). The table below describes the behaviour of the switches that control the RS232/485 interface.

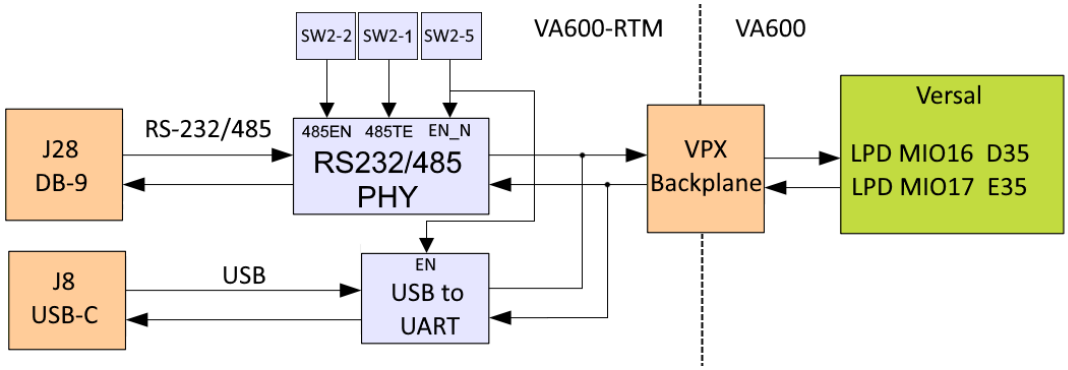


Figure 6 : Versal UART Diagram

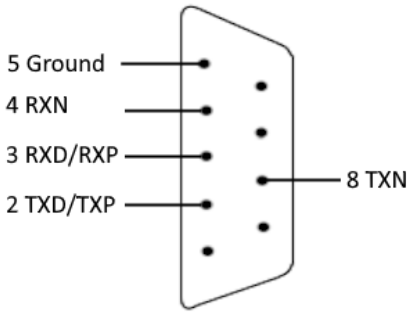


Figure 7 : Versal RS232/RS485 Pinout

Switch Ref.	Function	FPGA Pin	ON State	Off State
SW2-1	VA600 UART RS485 TE	K17	VA600 UART RS485 Termination Enable	VA600 RS485 Termination Disable
SW2-2	VA600 UART RS485 EN	J17	VA600 UART RS485 Mode	VA600 UART RS232 Mode
SW2-5	VA600 USB-to-UART EN	-	VA600 USB-to-UART enabled (RS232/485 disabled)	VA600 USB-to-UART disabled (RS232/485 enabled)

Table 7 : SW2 RS232/485 Definitions

3.2.5 JTAG Interface

3.2.5.1 On-board JTAG Interface

A JTAG boundary scan chain is connected to either an on-board USB to JTAG converter, or 14-pin JTAG header J29. This allows the connection of a Xilinx JTAG cable for FPGA debug using the Xilinx tools. The on-board USB to JTAG converter is enabled whenever a USB connection is made.

The scan chain is shown in JTAG Boundary Scan Chain:

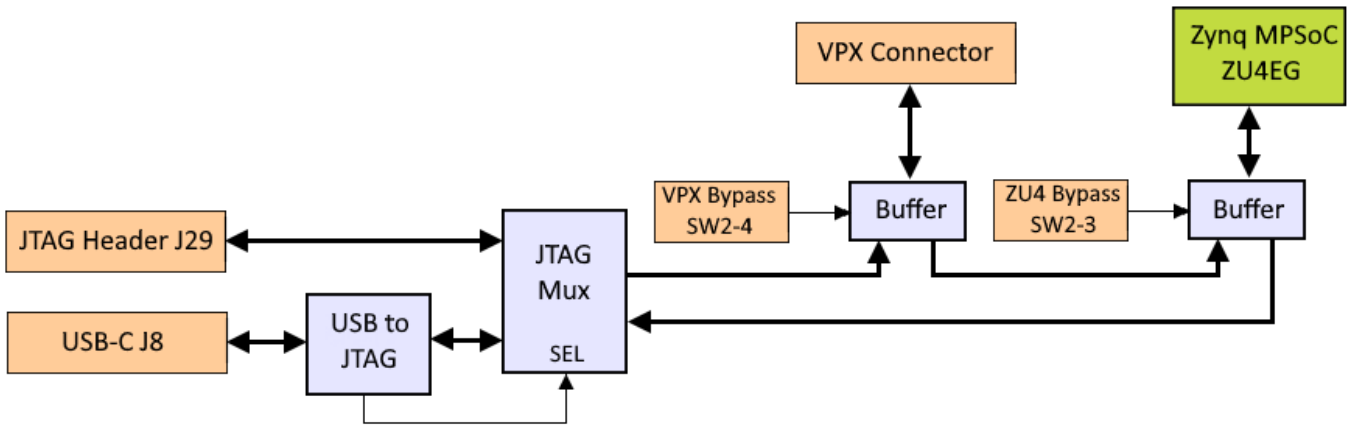


Figure 8 : JTAG Boundary Scan Chain

SW2-4 can be turned on to remove the VPX connector from the JTAG chain, leaving only the ZU4EG, and SW2-3 can be turned on to remove the ZU4EG from the JTAG chain, leaving only the VPX connector

3.2.5.2 JTAG Voltages

The on-board JTAG scan chain uses 3.3V. The VCC supply provided on J29 to the JTAG cable is +3.3V and is protected by a poly fuse rated at 350mA.

The JTAG signals at the VPX interface use 3.3V signals and are connected through level translators to the on-board scan chain.

3.2.6 High-Speed Debug Port (HSDP)

The VA600-RTM is compatible with the AMD SmartLynq+ JTAG cable, allowing 10Gb/s serial data transfer between the SmartLynq+ and the Versal device. The SmartLyqn+ supports JTAG, UART and HSDP over a single USB-C connection. The diagram below shows the full UART/JTAG/HSDP circuit:

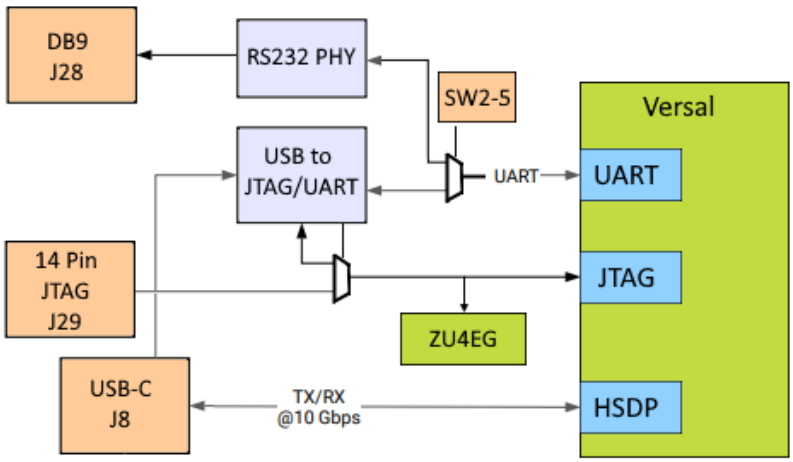


Figure 9 : JTAG Boundary Scan Chain

3.2.7 SpaceWire

There are two spacewIre connectors, each of which contains 4 differential pairs. The differential pairs are driven by single-ended to differential converters on the VA600 board, so the P and N diff parts are shown as going to the same Versal pin in the table below. These signals use LVDS signalling levels, and can accept a -4V to +5V common mode voltage range.

Connector	SpaceWire Pin	VA600 Versal Pin	Function
SpaceWire 1 J38	1	L37	DIN_P
SpaceWire 1 J38	6	L37	DIN_N
SpaceWire 1 J38	2	M34	SIN_P
SpaceWire 1 J38	7	M34	SIN_N
SpaceWire 1 J38	3	-	GND
SpaceWire 1 J38	9	M36	DOUT_P
SpaceWire 1 J38	5	M36	DOUT_N
SpaceWire 1 J38	8	K33	SOUT_P
SpaceWire 1 J38	4	K33	SOUT_N
SpaceWire 2 J39	1	N34	DIN_P
SpaceWire 2 J39	6	N34	DIN_N
SpaceWire 2 J39	2	M35	SIN_P
SpaceWire 2 J39	7	M35	SIN_N
SpaceWire 2 J39	3	-	GND
SpaceWire 2 J39	9	L33	DOUT_P
SpaceWire 2 J39	5	L33	DOUT_N
SpaceWire 2 J39	8	K37	SOUT_P
SpaceWire 2 J39	4	K37	SOUT_N

Table 8 : SpaceWire Pinout

3.3 Clocks

The VA600-RTM provides a variety of clocking options using fixed oscillators. These clocks can be combined with the FPGA's internal PLLs to generate a range of frequencies.

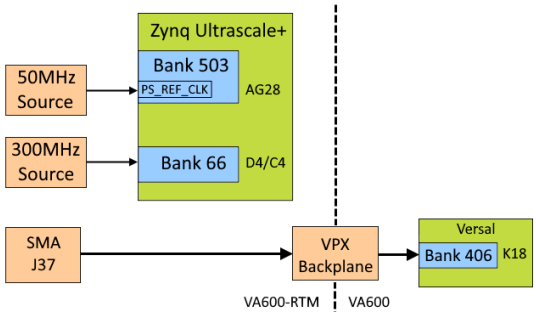


Figure 10 : Board Clock Diagram

3.3.1 300MHz Reference Clock

The fixed 300MHz reference clock REFCLK_300M is a differential LVDS signal.

REFCLK_300M is used as the reference clock for the PL and can be used as a reference for the IO delay control block (IDELAYCTRL).

Signal	Frequency	FPGA Input	IO Standard	"P" pin	"N" pin
REFCLK_300M	300 MHz	IO_L11_T1U_N8_GC_66	LVDS	D4	C4

Table 9 : 300MHz Connections

3.3.2 PS Reference Clock (PS_REF_CLK)

A 50MHz PS reference clock is provided for the ZU4EG processing system

Signal	Frequency	FPGA Input	IO Standard	FPGA pin
PS_REF_CLK	50 MHz	PS_REF_CLK	LVCMOS33	R16

Table 10 : PS_REF_CLK Connections

3.4 Zynq PS Block

3.4.1 Boot Modes

BootMode0 (SW1-1)	BootMode1 (SW1-2)	BootMode2 (SW1-3)	BootMode3 (SW1-4)	Boot Mode
ON	ON	ON	ON	JTAG
OFF	OFF	ON	ON	SD Flash
-	-	-	-	Reserved

Table 11 : Boot Mode Selection

3.4.2 MicroSD Flash Memory

A MicroSD card is used for storing executable code and data for the PS and PL, such as a bootloader, operating system and bitstream.

The SD Card can only be accessed by the PS.

3.4.3 PS DDR4 Memory

The VA600-RTM is fitted with one bank of PS DDR4 SDRAM. The bank is made up of a two 16-bit wide memory devices in parallel to provide a 32-bit data-path capable of running up to 1200MHz (DDR4-2400). 2GByte devices (Micron MT40A1G16RC-062) are fitted as standard to provide 4GByte of memory.

Full details of the interface and PS configuration example design are provided in the VA600-RTM example design.

3.4.4 I2C Interface

The on-board I2C devices are connected to an I2C bus from the PS of the ZU4EG. Devices that don't have individual I2C enables (SFF/SFP connectors) use an I2C buffer with an enable pin. These enable signals are drive by the PS and each have a pull-down resistor so they are disabled by default.

The I2C interface can be accessed from the PS. The Alpha Data example design PetaLinux image includes i2c utilities such as i2cdetect, i2cget and i2cset.

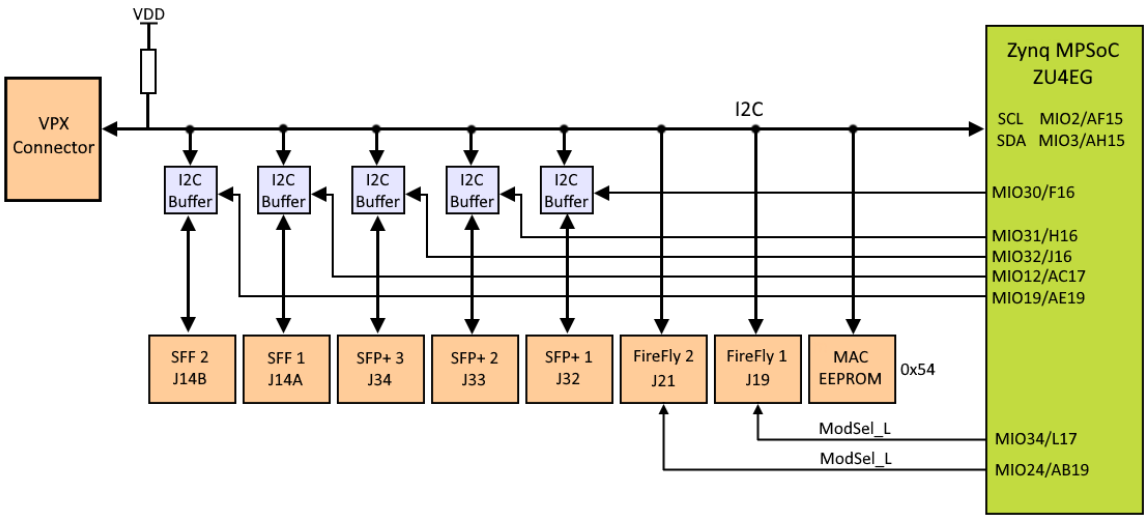


Figure 11 : VA600-RTM I2C Diagram

3.4.5 Ethernet Interfaces

The **VA600-RTM** has one 1000BASE-T Ethernet interface.

The interface has a Marvell 88E1512 PHY, connected to the Zynq via RGMII.

The interface has three status LEDs. The functions of these are shown in Table 12 below.

Eth0 LED	Eth1 LED	Colour	Function
D12	D19	Green	On = Link up
D7	D17	Green	Unused
D6	D14	Amber	On = Link up

Table 12 : Ethernet Status LEDs

3.4.6 Serial COM Port

There is one PS COM port connected to an on-board USB to serial converter. This USB to serial converter has a dedicated USB-C port that is separate from the Versal UART/JTAG connector.

3.4.7 USB Interface

The VA600-RTM has an external USB interface. The Zynq PS is configured as the USB host to the external interfaces.

3.5 PL Interfaces

3.5.1 I/O Bank Voltages

The FPGA IO is arranged in banks, each with their own power supply pins. The bank numbers, their voltage and function are shown in FPGA IO Banks. Full details of the IOSTANDARD required for each signal are given in the xdc constraints files of VA600-RTM example designs.

IO Banks	Voltage	Purpose
500, 501, 503	3.3V	Configuration, JTAG, Boot Mode Select, PS MIO
43, 44, 45, 46	3.3V	Single Ended GPIO, Board Control, SMAP
66	1.8V	Diff. IO, Board Control

Table 13 : FPGA IO Banks

3.5.2 PL GPIO

There are 37 single ended GPIO pins from the FPGA to the VPX backplane. These connect to the Versal MIO pins and can be used as a 32-bit wide SMAP interface. There are also 37 GPIO pins between the FPGA and external SMAP connector J10, which can be used to pass the SMAP through the FPGA, for example if an external device is used to control the SMAP interface.

There is also a reset signal that can be driven by the ZU4EG to assert the Versal power-on reset, as the SMAP clock must be running when the Versal POR is released.

Mating cable is Samtec SQCD-025-XX.XX-TEU-TEU-3, where XX.XX is the cable length in inches. See https://www.samtec.com/products/sqcd for details.

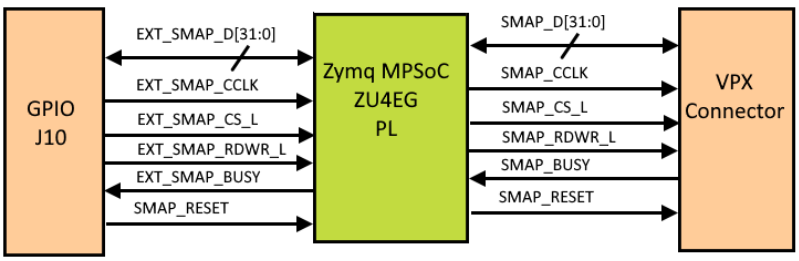


Figure 12 : SMAP IO Diagram

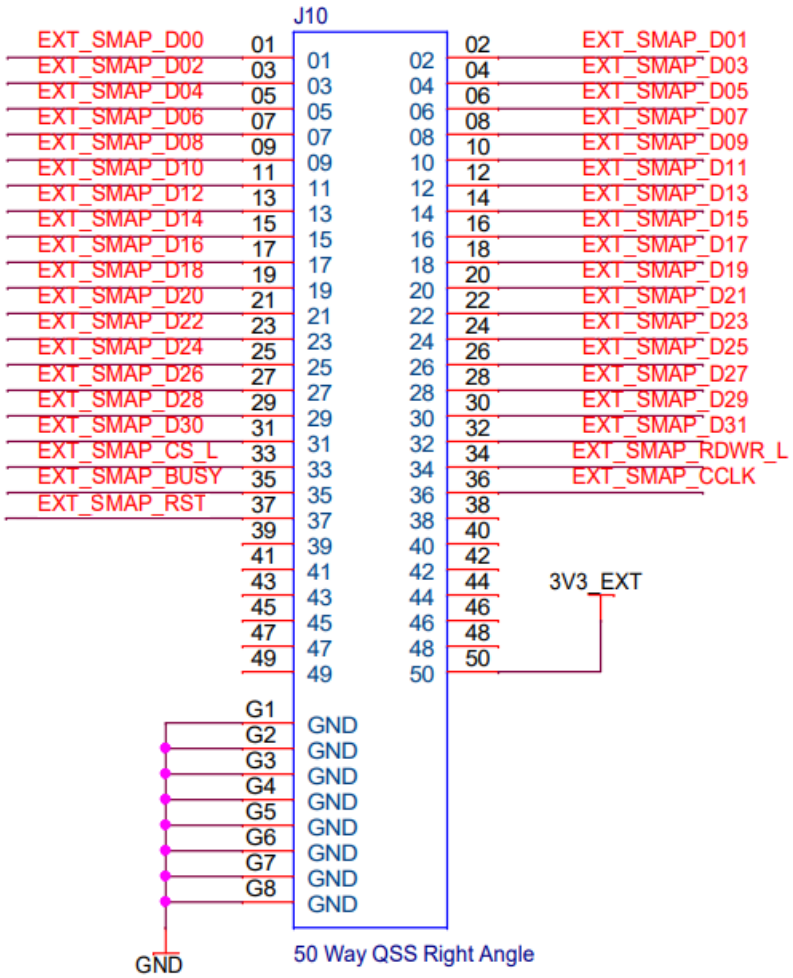


Figure 13 : SMAP Connector Pinout

3.6 Configuration

3.6.1 Power-Up Sequence

At power-up, the PS will load the first-stage bootloader from the memory interface selected by the Boot Mode select switches.

The first stage bootloader is responsible for configuring the FPGA and PS attached interfaces.

3.7 System Monitoring

The Zynq MPSoC on the VA600-RTM has the ability to monitor temperature and voltage to maintain a check on the operation of the board.

Control algorithms within the microcontroller automatically check line voltages and on board temperatures. The Zynq can monitor it's own power rails and temperatures. Supplies not monitored by the Zynq Sysmon are connected (though a resistor divider) to the Zynq's ADC blocks.

Rail	Scaling Factor	'P' Pin	'N' Pin	Purpose
VPX_12V	0.077	B4	A4	Board Input Supply
5V0	0.167	G8	F7	5V Rail, internally generated
2V5	0.667	E9	D9	2.5V Rail, internally generated
VTT_DRAM	1.0	C6	B6	0.6V DRAM Termination
1V2_PSPLL	0.5	C8	B8	1.2V PS PLL Voltage

Table 14 : Zynq ADC inputs

4 Example Design

A set of Vivado example designs, pinout/constraint files and Petalinux BSP are available at https://alpha-data.sharefile.com

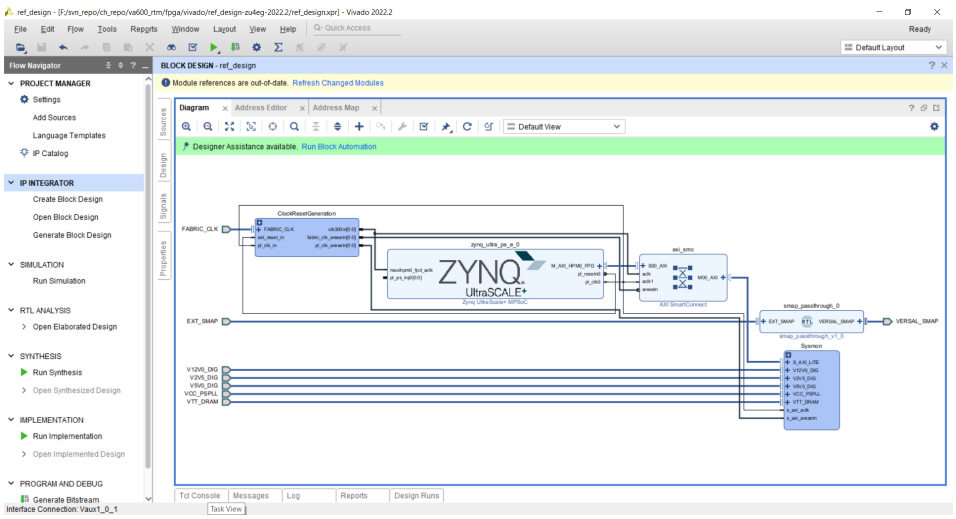


Figure 14 : VA600-RTM Example Design

Revision History

Date	Revision	Nature of Change
20th June 2023	1.0	First Release
21st August 2023	1.1	Added board weight
9th November 2023	1.2	Fixed SW2/SW1 reference mix up, added missing SW2 switches to RS232/RS485 diagram.

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